Bluetooth™ Radio

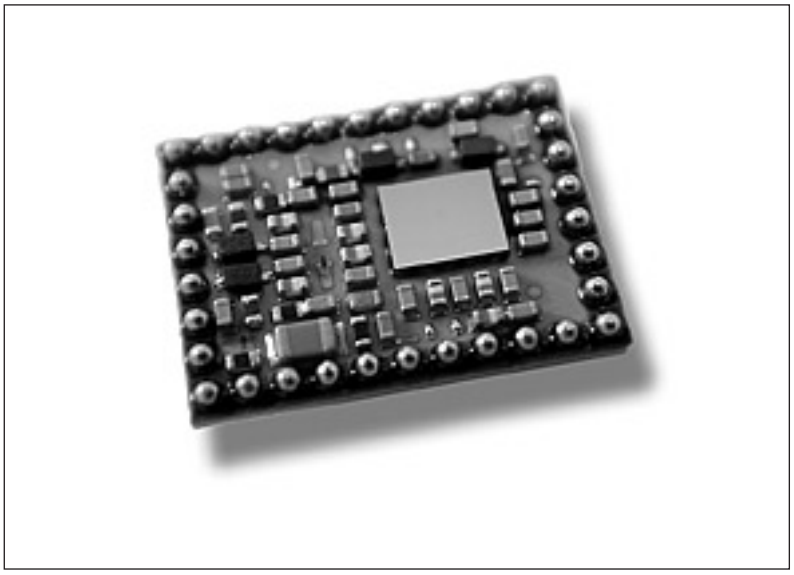
PBA 313 01/2 (Bluetooth 1.0b), PBA 313 01/3 (Bluetooth 1.1)

Key Features

- RF output power Class 2
- Compliant to Bluetooth specification 1.0b or 1.1
- Forms a complete radio with:
  - an antenna
  - a crystal or existing 13 MHz reference frequency
  - data and digital control circuitry (baseband)
- Small outline BGA-package (10.2 x 14.0 x 1.6 mm)
- Requires no external shielding

Suggested Applications

- Mobile phones, PDA, Modems, Laptop computers, Handheld equipment



Description

PBA 313 01 is a short-range microwave frequency radio transceiver for Bluetooth communication links that are designed to operate in the globally available ISM frequency band, 2.4-2.5 GHz.
Fast frequency hopping (1600 channel hops/s) with 79 channels available (2.402 to 2.480 GHz) and a maximum TX & RX bit rate of 1 Mbit/s exploits the maximum channel bandwidth allowed in the unlicensed ISM band. The implemented modulation technique is GFSK (Gaussian Frequency Shift Keying), with a BT product of 0.5.
The design is based around a BiCMOS ASIC mounted on a LTCC (Low Temperature Co-fired Ceramic) substrate. The antenna filter, R_X and T_X baluns are all integrated into the substrate. Connection to the PCB is achieved by a non-collapsing BGA structure which gives a self-shielding design.

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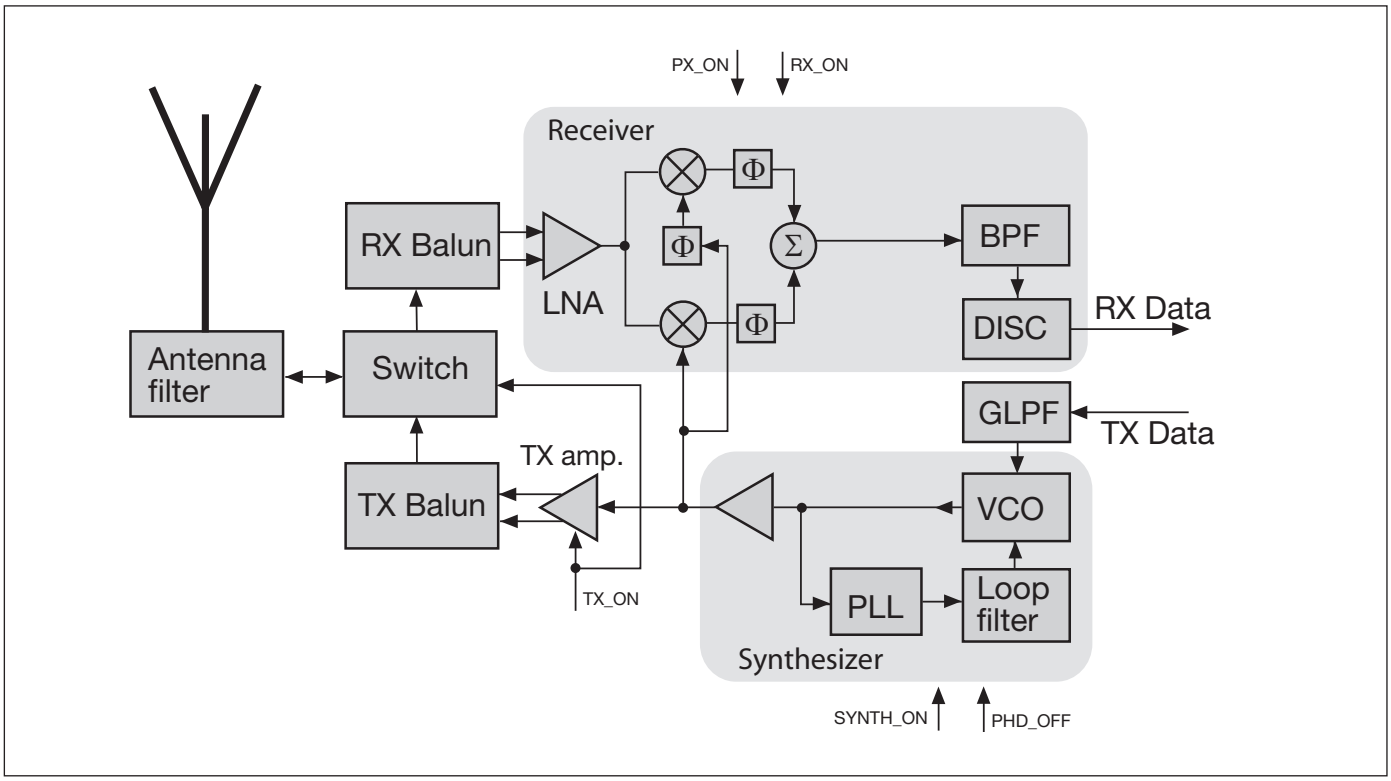


Figure 1. Block diagram.

Absolute Maximum Ratings

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}			+3.3	V
Applied voltage to non supply pins			-0.3		V_{CC} +0.3	V
Input RF Power	In-band				15	dBm
	Out-band				15	dBm
Storage temperature		T_{Stg}	-25		+100	°C

Recommended Operating Conditions

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Reference clock frequency	1), 2)	f_{EXT_CLK}	12.99974	13	13.00026	MHz
Reference clock amplitude			0.2		0.5	V
Reference clock phase noise Δf = 15 kHz					-110	dBc/Hz
Supply voltage		V_{CC_VCO}	2.7	+2.8	3.0	V
Applied voltage to non-supply pins			-0.3		V_{CC}+0.3	V
Output matching of ANT pin		$VSWR_{TX}$			2:1	
Antenna load				50		Ω
Logical input high		V_{IH}	0.9xV_{CC}		V_{CC}+0.3	V
Logical input low		V_{IL}	-0.3		+0.3	V
Rise/Fall time of all digital inputs			2		20	ns
Clock frequency of SI_CLK		f_{SI_CLK}			4	MHz
Positive period of SI_CLK		t_{SI_CLK2}	76			ns
Ambient temperature		T_{Amb}	-10	+23	+75	°C

1) If an external clock input is used the external clock should be AC coupled into the XO_N input and the XO_P input shall be left unconnected.

2) The load capacitance on the XO_N input can be trimmed by ±4 pF to allow frequency trimming when a crystal is used. Refer to the Design Considerations section for details on using the XO-trim register.

Electrical Characteristics

DC and low frequency Specifications

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Current consumption	Sleep mode[3]			65	200	µA
	SYNT_ON only			21	30	mA
	Receive mode			40	52	mA
	Transmit mode			32	44	mA
XO_N input capacitance	[4]	C_{XO_N}		11.5		pF
XO_P output capacitance				33		pF
Capacitance of all digital inputs				7		pF
Input leakage current	$0.5 < V_{IN} < (V_{CC} - 0.5)$			5		µA
Rise/Fall time of digital outputs	driving a 10 pF load			5		ns
Logical output high		V_{OH}		2.8		V
Logical output low		V_{OL}		0		V
SYS_CLK frequency				f_{EXT_CLK}		MHz
TX_CLK frequency				f_{EXT_CLK} /13		MHz
Minimum LPO_CLK frequency	[5]			2.0	3.1	kHz
Maximum LPO_CLK frequency			3.3	4.7		kHz

[3] Average after steady state.

[4] The XO_N input capacitance can be trimmed by ±4 pF by writing a 6-bit value to the XO-Trim register. Refer to the Design Considerations section for further information.

[5] If used, the baseband must trim LPO_CLK to 3.2 kHz by writing to the LPO trim registers in the radio. Refer to the Design Considerations section for further information.

RF Specifications (-10°C - T_A - +55°C, V_{CC} = 2.8 V, external frequency = 13 MHz ±10 ppm, matching of antenna, max $VSWR_{RX}$ = 2:1. Recommended value in register according to table 5.) Radio performance without baseband.

Parameter	Condition	Symbol	Min	Typ	Max	Unit
General						
Frequency range		f_{Range}	2.402		2.480	GHz
Input and output impedance of ANT pin				50		Ω
Receiver Performance (BER - 0.1%)						
Sensitivity level	75 kHz offset (max), f_{MOD}: 160kHz	$P_{In, Min}$			-71.5	dBm
Sensitivity level	0 kHz offset			-78		
Max input level	75kHz offset (max), f_{MOD}: 160kHz	$P_{In, Max}$	0	15		dBm
C/I (f_C = 2441 MHz)	C -4MHz [7], [8]			-37	-17	dB
	C -3MHz [7], [8]			-40	-17	dB
	C -2MHz [6], [7]			-24	-17	dB
	C -1MHz [6]			-5	+4	dB
	Co-channel [6]			+7	+14	dB
	C +1MHz [6]			0	+4	dB
	C +2MHz [6], [7]			-33	-17	dB
	C +3MHz [7], [8]			-41	-17	dB
	C +4MHz [8]			-43	-40	dB
C/I Blocking, DC - 5 GHz	see figure 3					
Out-of-band blocking	30-1910 MHz		+4	+13		dBm
	1910-2000 MHz		-10	+9		dBm
	2000-2399 MHz		-27			dBm
	2484-2999 MHz		-27	-14		dBm
	3000-3019 MHz		-11	-5		dBm
	3.00-12.75 GHz		-10	-5		dBm
Intermodulation characteristics			-39	-32		dBm
Spurious Emissions	30 MHz – 1 GHz				-57	dBm
	1 GHz – 12.75 GHz			-60	-47	dBm

[6] Carrier signal level at -60 dBm, interferer Bluetooth modulated.

[7] Exception allowed in Bluetooth test specifications.

[8] Carrier signal level at -67 dBm, interferer Bluetooth modulated.

RF Specifications, cont.

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Transmitter Performance						
Frequency modulation	Deviation from center frequency[9)]	f_{Mod}	140	155	175	kHz
Initial frequency error	[10)]		-75	0	+75	kHz
TX power			-4		4.5	dBm
TX carrier drift	1 slot (366 µs)	f_{Drift1}	-25		25	kHz
	3 slots (1598 µs)	f_{Drift2}	-40		40	kHz
	5 slots (2862 µs)	f_{Drift3}	-40		40	kHz
20 dB bandwidth	Measured with RBW: 10 kHz and peak detector			600	1000	kHz
Spurious Emissions	30 MHz – 1GHz				-36	dBm
	1 GHz – 12.75 GHz				-30	dBm
	1.8 GHz – 1.9 GHz				-47	dBm
	5.15 GHz – 5.3 GHz				-47	dBm

9) $f_{Mod} = (F_{Mod1}-F_{Mod0})/2$.

10) The initial frequency is mainly affected by the tolerance of the reference frequency or crystal; for every 1Hz deviation from 12MHz, the TX carrier offset is altered by approximately 186Hz.

C/I Blocking

The blocking characteristics can be basically split into two regions: In-band and Out-of-band. Blocking is performed both on the chip and on the module level.

- **Out-of-band**

– Antenna filter, DC to 1.9 GHz and 3:rd harmonic.
- Switch, low freq. and 2:nd harmonic.
- RX-balun, low freq. and 2:nd harmonic.
- On-chip IF filter.

Figure 2 shows the combination blocking effect of the antenna switch, antenna filter and RX balun. In addition to the blocking characteristics shown in figure 2, there is antenna isolation and filtering on the chip. Marker 1 shows the region where the Bluetooth band is located. Markers 2 - 4 show the blocking at the telecom frequency bands.
An example of total blocking characteristics can be seen in figure 3.

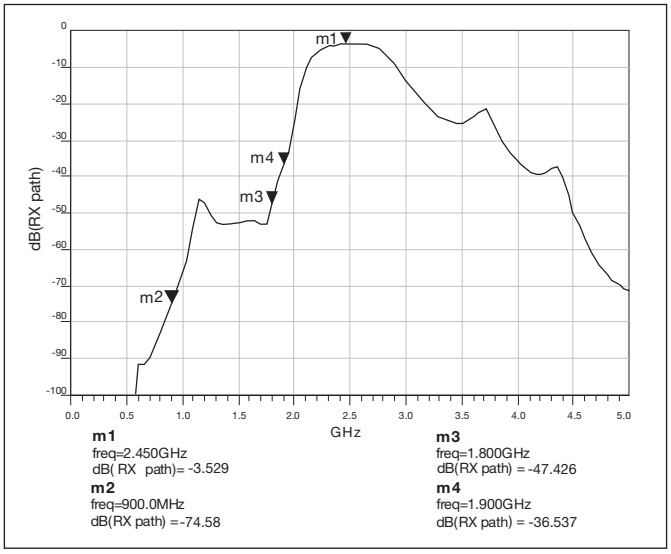


Figure 2. Typical out-of-band blocking characteristics excluding antenna isolation and on chip filtering.

Example 1	**Example 2**
Interferenc e of +33 dBm a t 2015 MHz.	Interferenc e of +33 dBm a t 1910 MHz.
• Antenna isolation 15 dB • Antenna filter, Antenna switch, RX-balun 27 dB	• Antenna isolation 25 dB • Antenna filter, Antenna switch, RX-balun 36 dB
• Interference level before IF filter +33-15-27= -9 dBm	• Interference level before IF filter +33-25-36= -28 dBm
0.1% BER requires a C/I of more than -40 dB at the IF filter.	
• 0.1% BER carrier level -40 + (-9)= -49 dBm	• 0.1% BER carrier level -40 + (-28)= -68 dBm

Figure 3. Blocking examples.

Mechanical specifications

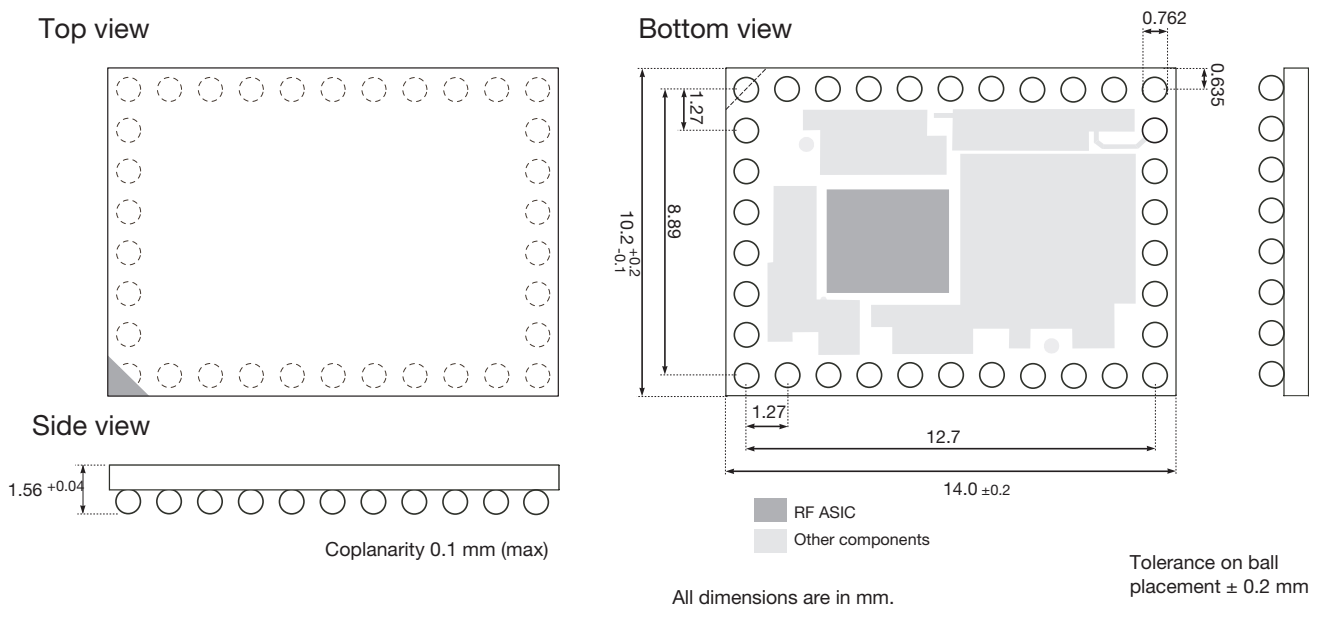


Figure 4. Mechanical dimensions of PBA 313 01.

Pin Description

Pin no.	Pin name	Type	Description
1	GND	Ground	Common ground
2	TX_CLK	D out	1 MHz clock
3	TX_ON	D in	Transmit power on
4	RX_DATA	D out	Received data output
5	RX_ON	D in	Receiver power on
6	GND	Ground	Common ground
7	XO_P	A in	Crystal positive output
8	XO_N	A in	Crystal negative input or external clock input
9	POR_EXT	D in	External power on reset
10	GND	Ground	Common ground
11	VCC	Power	Common power supply
12	GND	Ground	Common ground
13	GND	Ground	Common ground
14	GND	Ground	Common ground
15	GND	Ground	Common ground
16	GND	Ground	Common ground
17	ANT	50 Ω	Antenna input/output

Pin no.	Pin name	Type	Description
18	GND	Ground	Common ground
19	GND	Ground	Common ground
20	VCC_VCO	Power	VCO power supply
21	PHD_OFF	D in	Open PLL
22	TX_DATA	D in	Transmit data
23	GND	Ground	Common ground
24	SYNT_ON	D in	Synt power up
25	SI_CLK	D in	Serial interface clock
26	SI_CMS	D in	Serial interface control
27	SI_CDI	D in	Serial data input
28	GND	Ground	Common ground
29	SI_CDO	D out	Serial data output
30	POR	D out	Power on reset
31	LPO_CLK	D out	3.2 kHz clock
32	PX_ON	D in	Packet on
33	SYS_CLK_REQ	D in	System clock request
34	SYS_CLK	D out	System clock

Table 1. Pin description. * A = Analog, D = Digital

I/O Signal Description

Power supply

There are two connections to supply the Bluetooth radio with power. VCC_VCO supplies the sensitive VCO circuitry with power, and VCC is for the remaining circuitry. Each of the two supplies should be low frequency decoupled. See figure 13 for example circuitry.

Oscillator or external clock input

Refer to the Design Considerations section.
Oscillator or external clock input XO_N and XO_P connects to the crystal's inputs. The load capacitance to the crystal can be trimmed using the XO-Trim register. If an external clock is used, it should be AC coupled into the XO_N input and the XO_P input shall be left unconnected.

Antenna

The ANT pin should be connected to a 50Ω antenna interface, thereby supporting the best signal strength performance. Ericsson Microelectronics' partners can support application specific antennas.

Input Control

There are six digital inputs available for controlling the radio features of the PBA 313 01. The Bluetooth timing requirements for these are decribed in figure 6. In addition, there is a digital input signal for hardware reset of the radio, and a digital input signal for waking up the clock circuitry after a sleep mode period.

SYNT_ON

Synthesizer on control is active 'high'. Activate this signal to power up of the VCO section of the radio. SYNT_ON is used in both transmit and receive mode.

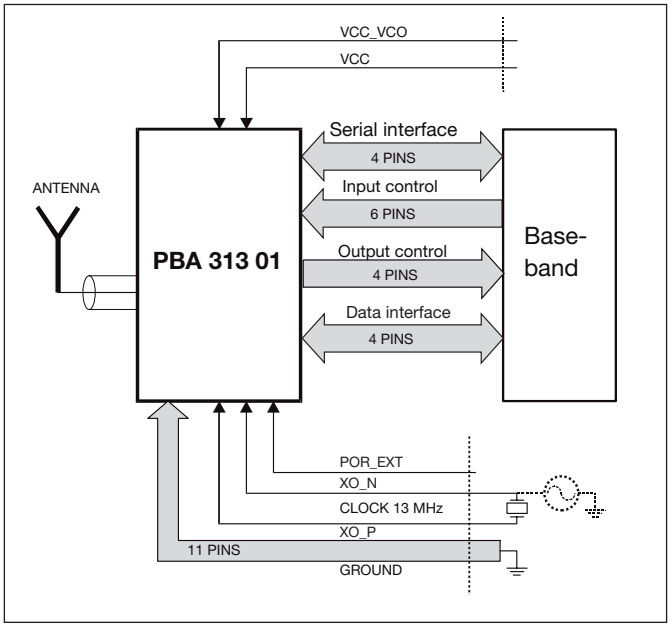


Figure 5. System overview.

RX_ON

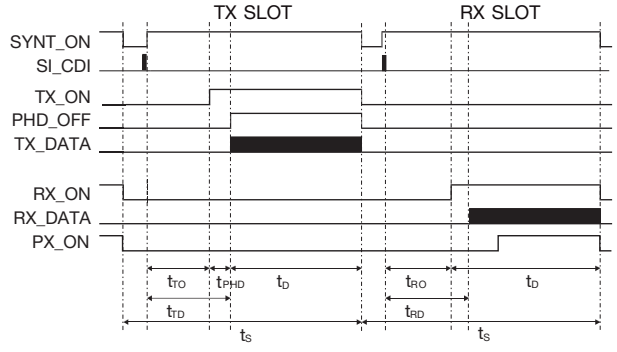
Receive-on control is active 'high'. Activate this signal to enable reception of Bluetooth data on the RX_DATA pin. The transmit-on control (TX_ON) must be deactivated and the synthesiser (SYNT_ON) activated if data is to be received.

PX_ON

Packet switch on control is active 'high'. Activate this signal during reception of a Bluetooth payload.
PX_ON is used to control the Dynamic Automatic Frequency Compensation (DAFC) of the receiver. Since the General Inquiry Access Code (GIAC), information in a Bluetooth packet header contains an equal number of one's (+FMOD) and zero's (-FMOD), the average frequency will always be centered on the carrier frequency. This provides the DAFC with the reference for the fast tuning. If the fast mode is not used during the header then the first bits could be interpreted incorrectly.
The slow mode gives a more accurate FSK compensation of the thresholds for a one and a zero compared to the fast mode; therefore, the BER is less. The fast mode (time constant <2µs) is used when PX_ON is deactived and the slow mode (time constant <50µs) when it is activated.

TX_ON

Transmit-on control is active 'high'. Activate this signal to enable radio signal output on the ANT pin. The actual transfer of data that exists on the TX_DATA input occurs when PHD_OFF goes 'high'. The receive-on control, RX_ON, must also be 'low' if data is to be transmitted.



Symbol	Parameter	Min	Typical	Max	Unit
t_S	One Slot time			625	µs
t_S	Two Slot times			1875	µs
t_S	Three Slot times			3125	µs
t_{TO}	Transmitter On delay		102		µs
t_{TD}	Delay before transmitting data	203	213	223	µs
t_{PHD}	Phase Detector Off delay after t_{TO}		104		µs
t_D	Data sending period, one slot			366	µs
t_D	Data sending period, two slots			1598	µs
t_D	Data sending period, three slots			2862	µs
t_{RO}	Receiver On delay		175	213	µs
t_{RD}	Delay before receiving data		213		µs

Figure 6 and table 2. Timing sequence for data transmission.

PHD_OFF

Phase detector off control is active 'high'. Activate this signal in transmit mode to open the phase locked loop (PLL) employed in the VCO synthesizer section and enable modulation of the carrier using the TX_DATA digital input. PHD_OFF is activated after the initialization of the SYNT_ON signal and the TX_ON signal, see figure 6 and table 2.

POR_EXT

External power on reset is active 'high'. An external power-on-reset digital input signal that will reset the radio controller and its registers. A reset will occur on the positive edge of POR_EXT signal.

SYS_CLK_REQ

System clock request control is active 'high'. Once the crystal oscillator bit (XOCTR, control register, bit #2) has been set, use this control to switch off (sleep mode) and wake up (idle and operating modes) the reference clock circuitry and corresponding 13MHz and 1MHz clock output ports of the module.

Output Control

There are four digital output control signals available for controlling external baseband circuitry.

POR

Power-on-reset digital output is activated after the power has been applied to the Bluetooth radio or on a positive edge of the POR_EXT digital input. POR has a transition from 'low' to 'high' after four clock cycles have been delivered to the baseband chip, see figure 7.

SYS_CLK

13 MHz system clock digital output available for the baseband circuitry when the POR_EXT and SYS_CLK_REQ are both 'high'. SYS_CLK will also be available during startup, independent on the value of SYS_CLK_REQ, see figure 7.

TX_CLK

1 MHz transmit clock digital output available for the baseband circuitry when the POR_EXT and SYS_CLK_REQ (see above) are both 'high'. TX_CLK changes value on rising edges of SYS_CLK.

LPO_CLK

3.2 kHz low power oscillator clock digital output that is adjustable by setting the internal LPOHI and LPOLO registers (see Design Considerations). The clock output is available as soon as the power supply is applied and POR_EXT is 'high' (figure 7). The LPO is necessary for wake-up timing in the baseband circuitry, if the Ericsson baseband is used. LPO_CLK must be trimmed to $^1/_2$ LSB from 3.2 kHz or calibrated within 230 ppm, using SYS_CLK or TX_CLK.

Data Interface

Two digital signals are used for data flow over the air interface.

TX_DATA

Transmit data digital control is active 'high'[12]. The radio module feeds Bluetooth data (1Mbit/s) directly to the radio frequency modulator when PHD_OFF is activated. The total delay from the TX_DATA pin to the ANT pin is typically 0.5µs.

RX_DATA

Receive data digital output is active 'high'. The radio module latches out Bluetooth data (1 Mbit/s) on the RX_DATA pin on each falling edge of SYS_CLK when RX_ON is activated. The total delay from the ANT pin to the RX_DATA pin is typically 2.5µs.

[12] Data on the TX_DATA pin is digitally buffered before it is fed to the radio frequency modulator. The polarity of this input can be set to normal by writing '1' or inverted by writing '0' to bit 0 of the Enable register.

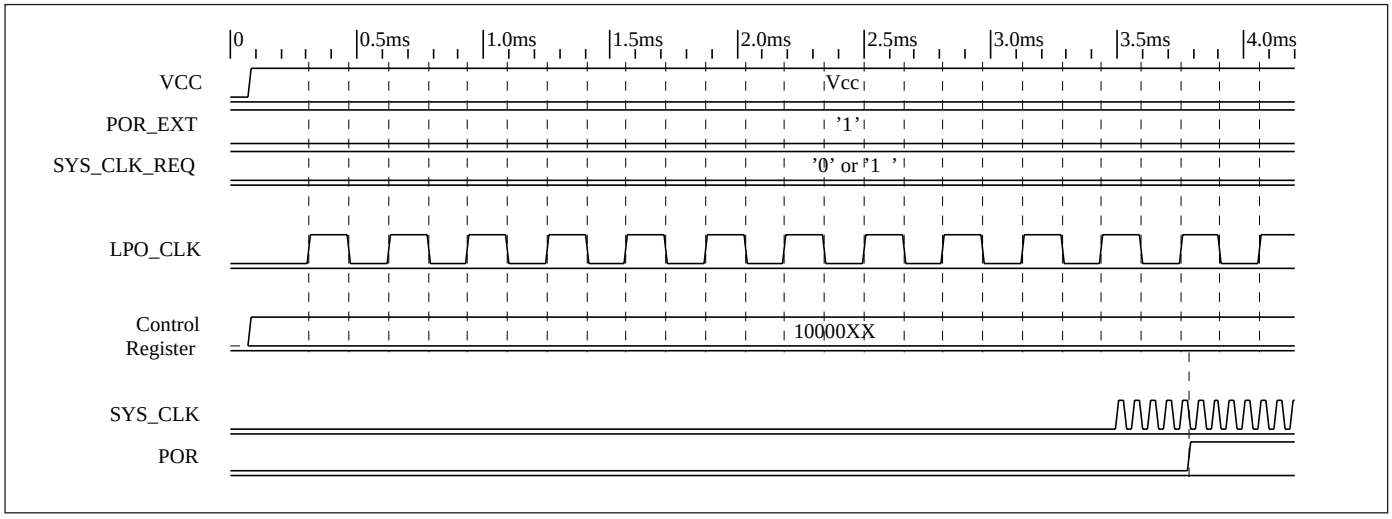


Figure 7. Powering up the module.

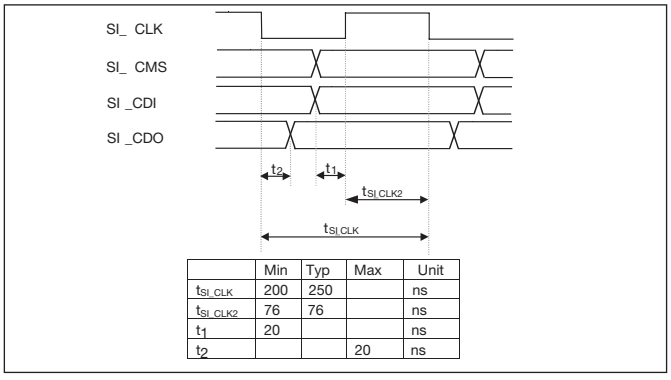
Serial Interface

The serial control interface is a JTAG Boundary-Scan Architecture (IEEE Std 1149.1). Interconnection between the serial interface and the external controller (baseband circuit) consists of four 1-bit digital signals; control data input (SI_CDI), control mode select (SI_CMS), control clock (SI_CLK) and control data output (SI_CDO). The timing of these signals are defined in figure 8.

State Diagram

The serial interface (SI) is operational when POR is 'high'. The state diagram is shown in figure 9. Transitions from one state to another depend on the SI_CMS input at the rising edge of SI_CLK. The SI controller is normally kept in the Run-Control/Idle state. SI_CMS and SI_CDI should change value at the falling edge of SI_CLK. The SI_CDO output will also change at the falling edge of SI_CLK.

Four types of instruction registers (table 3) can be accessed in an IR-Scan. Performing an IR-Scan with IR=01YYYY selects one of the data register in the radio. Reference source not found. IR starting with the bit code 11 allows serial data to be by-passed from SI_CDI to SI_CDO. The EXTEST and SAMPLE/PRELOAD instructions have no action.



	Min	Typ	Max	Unit
t_{SI_CLK}	200	250		ns
t_{SI_CLK2}	76	76		ns
t_1	20			ns
t_2			20	ns

Figure 8. Timing diagram of the serial interface.

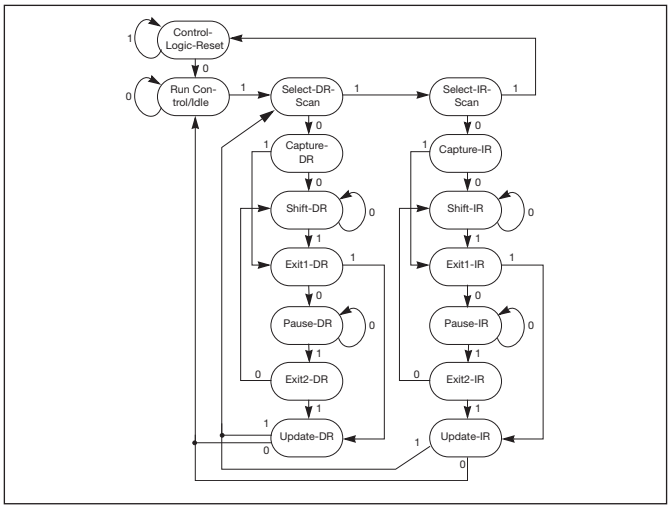


Figure 9. State machine for serial interface control. '0' denotes a logic level 'low' and '1' level 'high' level on the SI_CMS control pin.

IR	Description
00	EXTEST (no action)
01YYY	Selection of a Data Register
10	SAMPLE/PRELOAD (no action)
11	BYPASS

Table 3. Instruction registers.

Data register scans (DR-Scan) transfer 8 bits data from the readable register at address 01YYYY to SI_TDO, and 8 bits of data from SI_TDI to the writable register at the same address, in one single operation. See figure 10. Table 5 lists the different registers in the radio controller, their read or write operation, address, and content after a reset. The functionality is described in table 4.

Delay		
bit 7:	Delay PHD_OFF negative edge 6 us.	
bit 6:	Delay SYNT_ON negative edge 6 us..	
bit 5-3:	Reserved.	
Channel		
bit 7:	RX/TX	- Receive (1) or Transmit (0) channel
bit 6-0:	Channel value	- 0 - 127 decimal
RSSI		
bit 4-0:	Received signal strength indicator, lower input power gives lower RSSI value.	
XO-trim		
bit 5-0:	Trim value for the internal capacitor load of the crystal (0 = 0 pF, 63 = 8 pF)	
ID		
bit 7-4:	Chip identity, Radio Controller = 0001.	
bit 3-0:	Chip version number.	
LPOLO		
bit 7-0:	Eight least significant bits of the LPO frequency adjust value (LPO7-LPO0). LPO8:0 = 0 gives maximum fLPO and 511 mininum fLPO.	
LPOHI		
bit 0:	Most significant bit of the LPO adjust value (LPO8).	
Control		
bit 6-3:	LPO coarse trimming, lower value gives higher fLPO.	
bit 2:	Crystal oscillator control. After POR has been activated, a 0 to 1 transition enables the SYS_CLK_REQ control pin.	
Modulation		
bit 6-4:	TX modulation amplitude. 0 gives 10% higher than the nominal value, 7 gives 10% lower.	
bit 3-0:	Reserved.	
Current		
bit 7-5:	Reserved.	
Enable		
bit 7-6:	Reserved	
bit 5-1:	Amplifier power control. 00000=On, 11111=Off.	
bit 0:	Polarity of TX_DATA. 1 = positive, 0 = negative polarity.	

Table 4. Description of registers.

Register name	# bits	R or W	Address	Value at reset	Recommended value
VCO/DAFC/Delay	8	W	$010001_2 = 17_{10}$	00000X00	1111 $1011_2 = 251_{10}$
Channel	8	W	$010010_2 = 18_{10}$	00000010	
RSSI	5	R		XXXUUUUU	
XO-trim	6	W	$010011_2 = 19_{10}$	XX000000	
ID	8	R		0001VVVV	
LPO-hi	1	W	$010101_2 = 20_{10}$	XXXXXXX0	
LPO-lo	8	W	$010100_2 = 21_{10}$	00000000	
Control	7	W	$010110_2 = 22_{10}$	X10000XX	Bit two set to 1 to enable SYS_CLK_REQ
Modulation	8	W	$010111_2 = 23_{10}$	00000000	$0100\ 0000_2 = 64_{10}$
Current	3	W	$011000_2 = 24_{10}$	000XXXXX	$0000\ 0000_2 = 0_{10}$
Enable	8	W	$011001_2 = 25_{10}$	UUUUUUUU	$1011\ 1111_2 = 191_{10}$

W = Writable, R = Readable, X = Not applicable, U = Undefined, V = Version number

Table 5. Data registers in the radio controller.

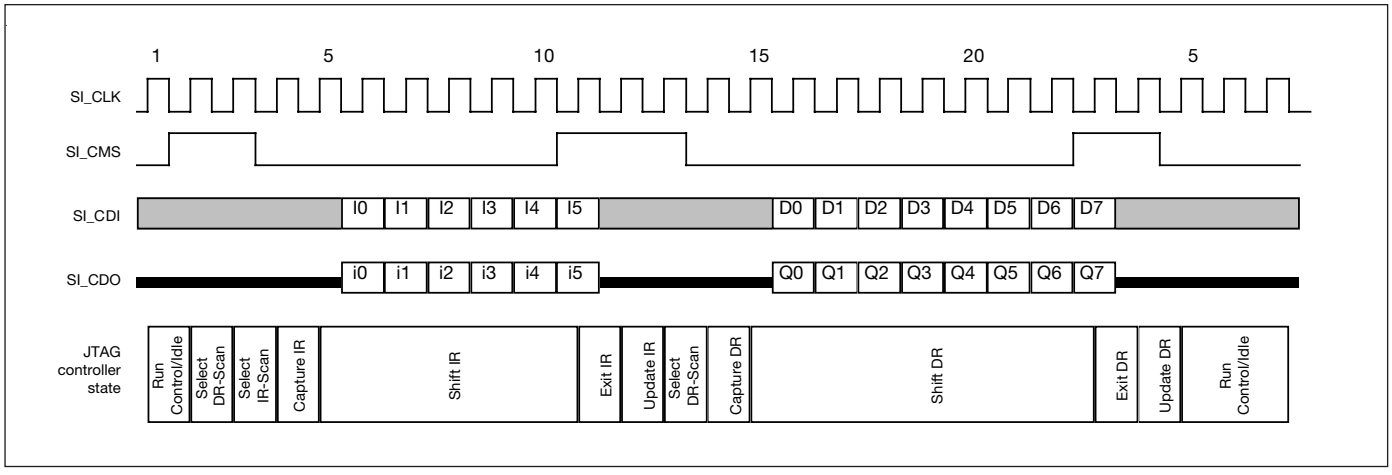


Figure 10. Reading and updating a data register. A data register is selected by entering the Shift IR state using SI_CMS, and transferring the appropriate bit code to the instruction register using SI_CDI (I[5:0]=01YYYY, where YYYY is the address of the register). Moving to the Shift-DR state, eight bits of register data can then be transferred on SI_CDI and SI_CDO. The data register selected by the instruction register is updated when the SI controller enters the Update-DR state. At the end of the data register access, the SI controller is once again held in the Run Control/Idle state.

Serial interface example

Writing the value 77 to the Channel register selects Bluetooth channel 75 (i.e. 2477 MHz) for transmission. This will simultaneously read the RSSI measurement for the latest received packet header. The normal operation sequence is:

- Point out the Channel register, this is done by performing an IR-scan. The SI_CMS signal should be controlled as shown in figure 10. When in the Shift-IR state the value 010010 should be shifted in on the SI_CDI input (LSB first). When in the Run Control/Idle state the Instruction Register is updated.
- Write the new channel value, this is done by performing a DR-scan. The SI_CMS signal should be controlled as shown in figure 10. When in the Shift-DR state, SI_CDI= 01001101 should be shifted in (LSB first). When in the Run Control/Idle state the Channel register is updated.

If no other register has been addressed then the Channel register contents are still in the IR, therefore only a new DR-scan needs to be done to change to another frequency channel.

Design Considerations

Power-up sequence

The start-up sequence is as follows, see figure 11 for typical timing:

1. The start-up sequence starts with a Power-On-Reset (POR_EXT) or by applying power to VCC. This resets all the registers in the radio controller.
2. The LPO_CLK starts to oscillate.

3. The 13 MHz clock circuitry stabilises and is output to the CLK_REF pin. POR is activated when four complete cycles have been delivered to the baseband.
4. The baseband should now initiate the XO-trim register, Control, Modulation and LPO registers. The XO-trim register should be set to the stored calibration value from the production calibration. The Control and Modulation register should be set to the recommended values for normal operation.
5. The LPO frequency must be adjusted to 3.2 kHz. This is done by comparing LPO_CLK with a fraction of the system clock frequency, SYS_CLK. The initial calibration of the LPO can use a successive approximation algorithm that adjusts the LPO register value from its mid value (256) in finer and finer steps until satisfied accuracy has been achieved. This compensates for oscillator frequency variations due to process variations of the resistors and capacitors. Thereafter, calibration of the LPO only has to be done due to temperature and voltage variations by increments or decrements of the LPO register value.
6. The Bluetooth radio and the baseband is now initialized up to the point that is normally called stand-by mode.
7. To activate the radio and be ready for transmission/ receive, write the value $11111011_2 = 251_{10}$ to the VCO/ DAFC control register and the value $10111111_2 = 191_{10}$ to the Enable register.
8. To enter sleep mode power down the crystal by resetting SYS_CLK_REQ. Bit 2 in the control register must be set to enable SYS_CLK_REQ.

Ground

Ground should be distributed with very low impedance as a ground plane. Connect all GND connections to the ground plane. It is critical to have a ground plane underneath the Bluetooth radio in order to shield the VCO tank from any electrical noise, see figure 12. The ground vias purpose is to connect the local ground plane to the main ground layer. Note: If a local ground plane cannot be directly placed underneath the radio, then no routing should be planned underneath the radio until a layer can be used as a local ground plane. The Bluetooth radio will be self shielding and no additional shields should be necessary for normal operating conditions.

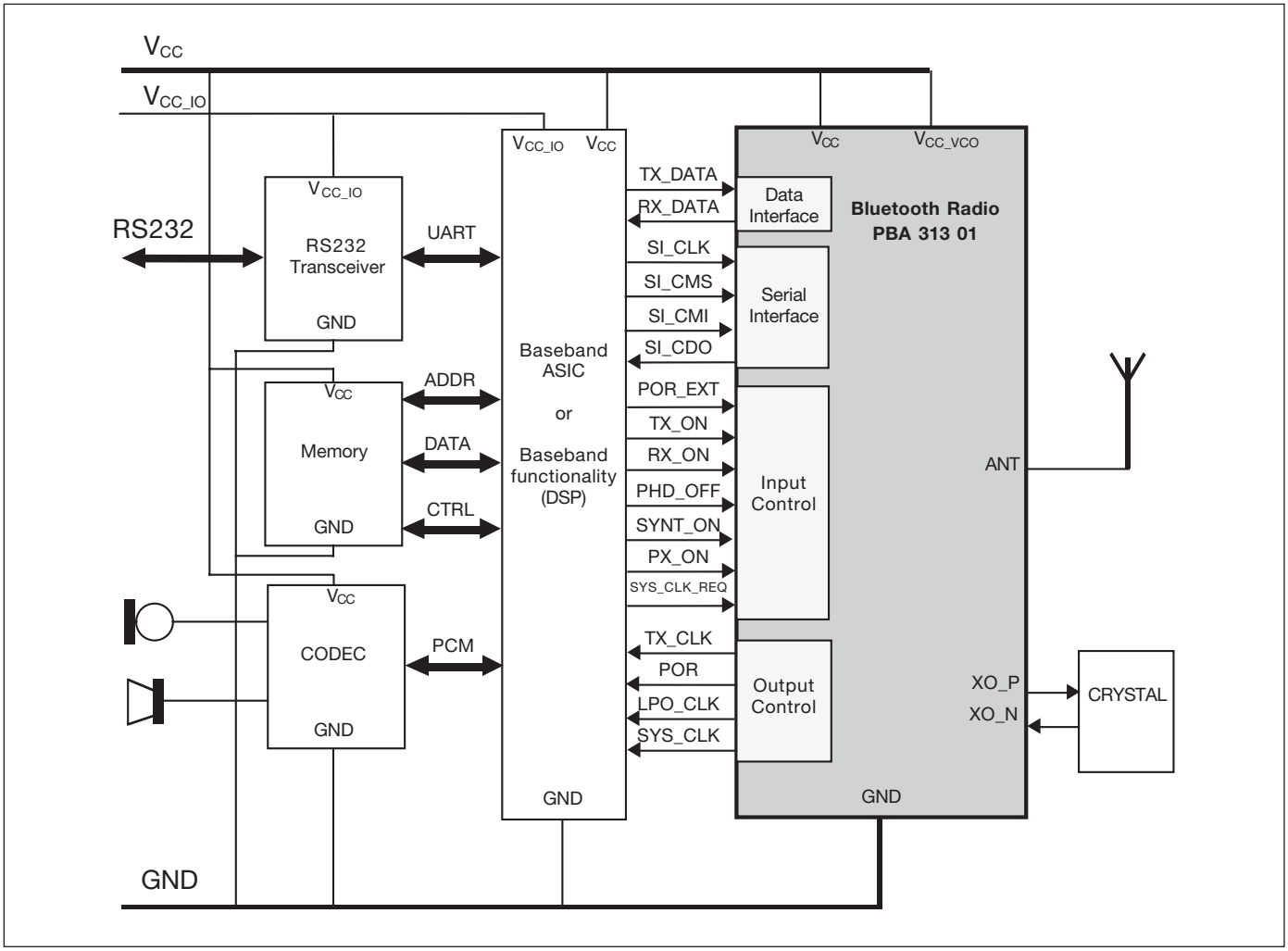


Figure 11. Typical UART or PCM configuration.

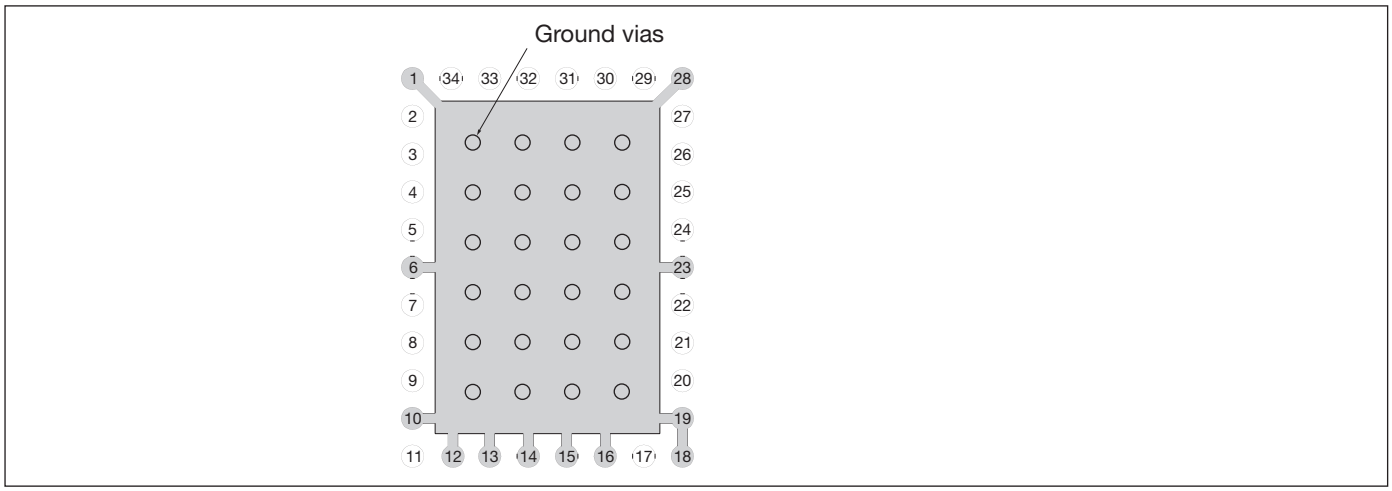


Figure 12. Example of local ground plane underneath the Bluetooth Radio.

Application schematic

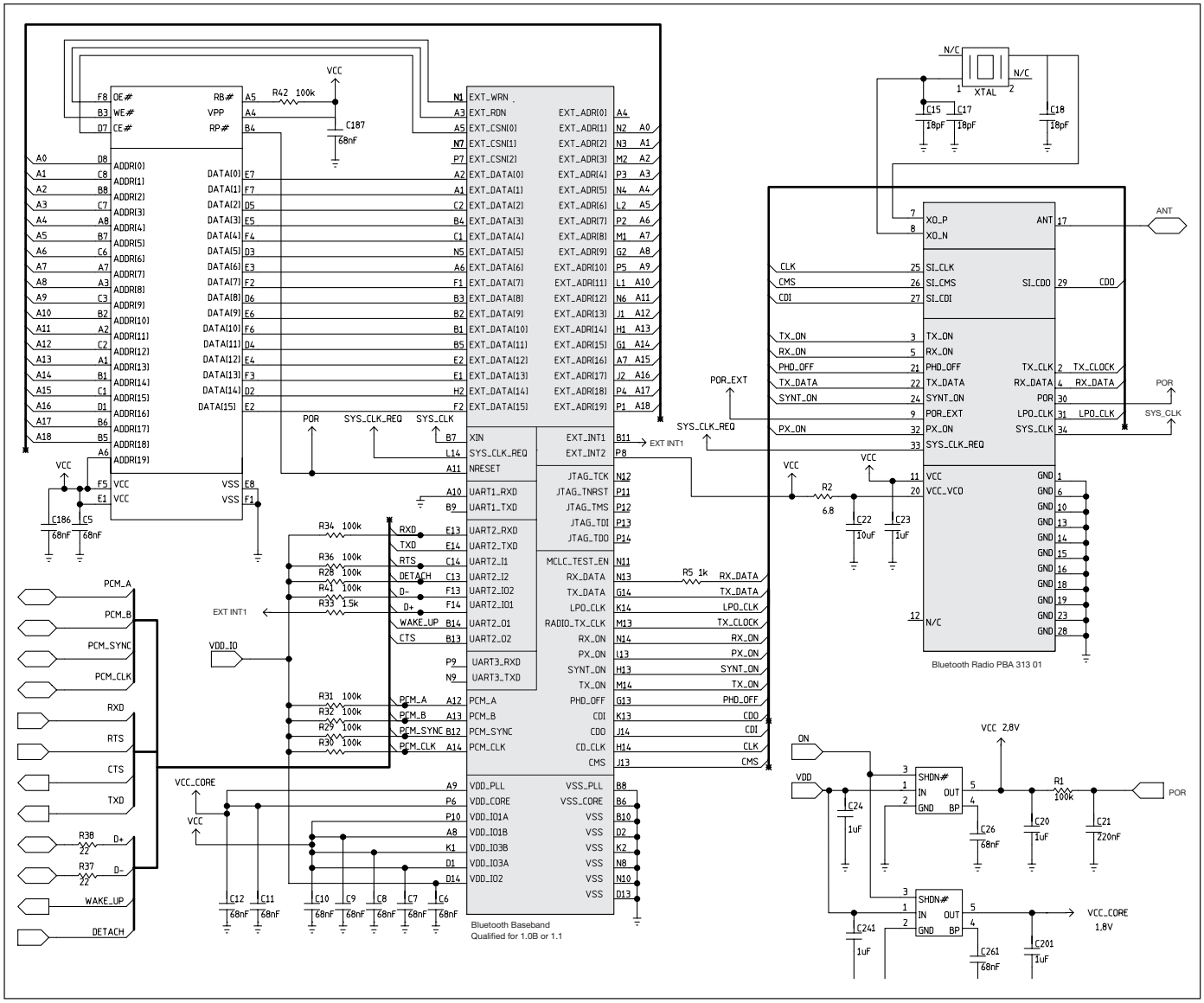


Figure 13. Example of interface between Ericsson Bluetooth Baseband and Bluetooth Radio.

Marking

Module marking

Each transceiver module is marked with the following information on the top side of the ceramic substrate (see figure 14):

a) Ericsson logotype.
b) Internal number.
c) Ericsson Microelectronics product number and version.
d) Manufacturing year and week, factory code and batch number.

Reel marking

Each reel is marked with the following information:

a) Ericsson logotype.
b) Internal number.
c) Ericsson Microelectronics product number and version.
d) Number of components on the reel.
e) Manufacturing year and week, factory code and batch number.

The marking is also printed in bar-code format.

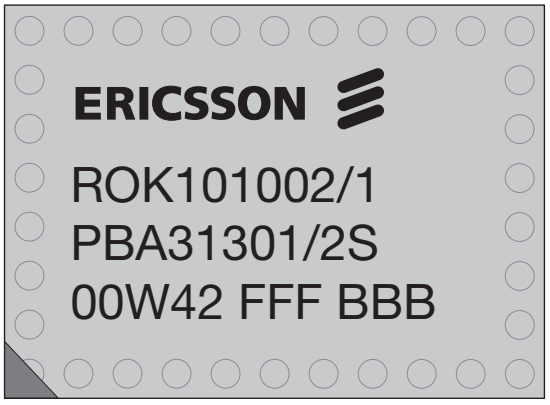


Figure 14. Top view with marking example and pin one indicator.

Packing

All devices will be delivered in tape & reel protecting them from electrostatic discharges and mechanical shock (see figure 15). The tape width is 24 mm and the component centre to centre distance is 16 mm. The size of the reel is 13". The number of parts per reel is 1500 units.

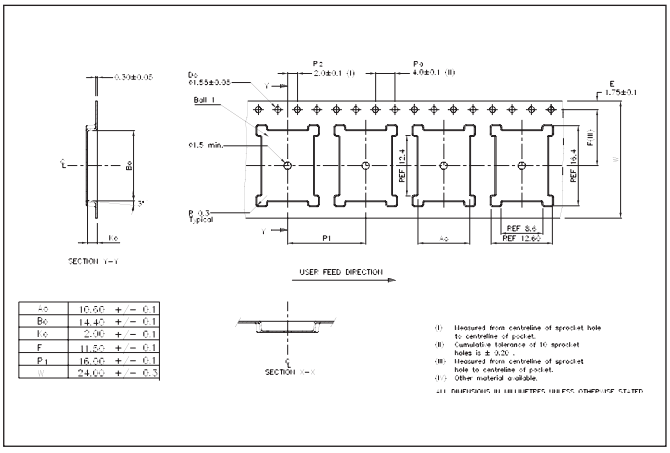


Figure 15. Carrier tape dimensions.

Ordering Information

BT Specification	Part No.
1.0b	PBA 313 01/2S
1.1	PBA 313 01/3S

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Preliminary Data Sheet

EN/LZT 146 65 R3B