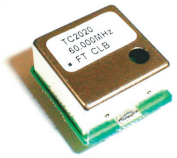

HIGH STABILITY TCXO/VCTCXO IN 20X20 mm METAL PACKAGE - TC2020 Series

FEATURES

- Stability to ±0.8 ppm / -20°C to 70°C
- Available Output: TTL, CMOS, Clipped Sine Wave
- Industry de factor Standard Pin Configuration
- Build to Order between 1.544 MHz to 120 MHz

SPECIFICATIONS

Frequency Range	1.544 MHz to 120 MHz (CMOS/TTL) or 9.60 MHz to 30 MHz (Clipped Sinewave)
Input Voltage (Vcc)	A = 5.0 VDC ± 5%; B = 3.3 VDC ± 5%
Input Current	30 mA Max. (CMOS/TTL) or 3.0 mA Max. (Clipped Sinewave)
Storage Temperature	-55°C to 125°C
Controllable Frequency Option	I = Internal trimmer only (no voltage control input): ±3 ppm Minimum
	VXI = Voltage control: ±5 ppm Min. + Internal Trimmer
Pull Range (X, Minimum)	5 = ±5 ppm (std.); 10 = ±10 ppm; 15 = ±15 ppm; 20 = ±20 ppm; 30 = ±30 ppm
Control Voltage (Vc)	2.5±2.0 VDC for Vcc = 5 VDC; 1.65±1.5 VDC for Vcc = 3.3 VDC
Setability of Vc at Fnom, 25°C	2.5±0.5 V DC for 5.0V part; 1.65±0.4 VDC for 3.3V part
Frequency Stability vs Temp	010 = ±1 ppm; 015 = ±1.5 ppm; 020 = ±2 ppm; 025 = ±2.5 ppm
Operatng Temperature Range	A = 0°C to 70°C; B = -40°C to 85°C; C = -10°C to 60°C; D = -20°C to 70°C
Frequency Stability vs Vcc	±0.3 ppm Maximum / Vcc ± 5%
Frequency Stability vs Load	±0.3 ppm Maximum
Aging	±1.0 ppm Maximum per year @25°C
Output	C = CMOS: 15 pF, 40/60% duty cyle, ± 3 dBm load
	T = TTL: 10 TTL, 40/60% duty cyle, ± 3 dBm load
	L = Clipped Sinewave: 20 KOhms/5 pF, 1Vp-p Minimum
SSB Phase Noise (Typical)	-80 dBc/Hz at 10 Hz
	-110 dBc/Hz at 100 Hz
	-135 dBc/Hz at 1 KHz
	-145 dBc/Hz at 10 KHz
Typical Part Number	TC2020-Frequency-Vcc-Controllable Freq. Option-Freq. Stability over Temp-Output
P/N Example	TC2020-60M000-AV15I010DT: CMOS output VCTCXO in 20x20x6 mm DIP metal package
	60.000MHz, 5V supply voltage, ±1 ppm / -20°C to 70°C, voltage tuning: ±15 ppm.

OUTLINE DRAWING