

HCMOS/TTL COMPATIBLE TRI-STATE VCXO IN 14 PIN DIP PACKAGE- VC14T Series

FEATURES

- Wide Frequency Pulling Range, 5 VDC or 3.3 VDC Option
- Very Low Phase Jitter with Fundamental Crystal Design
- Commercial or Industrial Temperature Range
- Hermetically Sealed 14-pin DIP Package with Industry Standard Lead Spacing

SPECIFICATIONS

Frequency Range	1 MHz to 39 MHz
Input Voltage (Vcc) Input Current Control Voltage (Vc) Storage Temperature	A = +5 VDC \pm 5%; B = +3.3 VDC \pm 5% 40 mA Maximum, depending on frequency and output load +2.5V \pm 2.0V for 5.0V part; +1.65V \pm 1.5V for 3.3V part -55°C to 125°C
Frequency Stability / APR (Min) Temperature Range Standard Stability / Pullability	A = $\pm 50 / \pm 50$ ppm; B = $\pm 25 / \pm 50$ ppm; C = $\pm 50 / \pm 100$ ppm A = 0°C to 70°C; B = -40°C to 85°C; C = -10°C to 60°C AA = ± 50 ppm / 0°C to 70°C, Absolute pull range (APR): ± 50 ppm Minimum
Duty Cycle Output Load Logic "1" / Logic "0" Level Rise/Fall Time (Tr/Tf) Start-up time Phase Jitter Modulation Bandwidth Linearity / Slope Input Impedance Setability at Fnom, 25°C Tristate Function Enable/Disable Time	1 = Tristate 60/40% symmetry; 3 = Tristate 55/45% symmetry HCMOS: drive up to 15 pF load; TTL: drive up to 10 TTL gates 0.9Vcc Minimum / 0.1Vcc Maximum 10 ns Maximum at 20% to 80% Vp-p 10 ms Maximum 1 ps Maximum at 1Sigma for fj > 1 kHz 10 kHz Minimum at -3 dB \pm 10% Maximum of best straight line fit / Positive 10 kOhms Minimum +2.5V \pm 0.5V for 5.0V part; +1.65V \pm 0.4V for 3.3V part Input (Pin 3) High (> 2.5V) or open: Output (Pin 8) active Input (Pin 3) Low (< 0.5V): Output disabled in high impedance 100 ns Maximum
Typical Part Number	VC14T-Frequency-Vcc-Freq. Stability/Pullability-Temperature Range-Duty cycle
P/N Example	VC14T-27M000-BAA3: HCMOS/TTL compatible tristate VCXO in 20.8x13x5 mm 14-pin DIP metal package, 27 MHz, +3.3 VDC, ±50 ppm / 0°C to 70°C, APR: ±50 ppm Minimum, Duty cycle: 55/45

OUTLINE DRAWING

