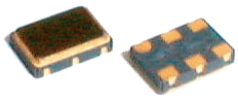

LV-PECL COMPATIBLE OUTPUT VCXO IN CERAMIC LCC PACKAGE - VC75PE Series

FEATURES

- RoHS Compliant (Pb-Free), High Frequencies
- Very Low Phase Jitter with Fundamental Crystal Design
- Leadless Chip Carrier Ultra Small Package with Industry de facto Standard Footprint
- Wide Frequency Pulling Range, No Internal PLL

SPECIFICATIONS

Frequency Range	130 MHz to 200 MHz
Input Voltage (Vcc)	B = +3.3 VDC ± 5%
Input Current	100 mA Maximum
Control Voltage (Vc)	+1.65V ± 1.5V
Storage Temperature	-55°C to 125°C
Frequency Stability / APR (Min)	A = ±50 / ±50 ppm; B = ±25 / ±50 ppm; C = ±50 / ±100 ppm; D = ±25 / ±75 ppm
Temperature Range	A = 0°C to 70°C; B = -40°C to 85°C; G = -10°C to 70°C
Standard Stability / Pullability	AA = ±50 ppm / 0°C to 70°C, Absolute pull range (APR): ±50 ppm Minimum
Duty Cycle	1 = Tristate 60/40% symmetry; 3 = Tristate 55/45% symmetry
Output Load	50 Ohms to Vcc - 2.0V or Thevenin equivalent, Bias required
Logic "1" / Logic "0" Level	Vcc - 1.02V Minimum / Vcc - 1.63V Maximum
Rise/Fall Time (Tr/Tf)	1 ns Maximum at 20% to 80% Vp-p
Start-up time	5 ms Maximum
Phase Jitter (RMS, 1 Sigma)	1 ps Maximum for fj = 12KHz to 20MHz
Modulation Bandwidth	12 kHz Minimum at -3 dB
Linearity / Slope	±20% Maximum of best straight line fit / Positive
Input Impedance	50 kOhms Minimum, fm < 10KHz
Setability at Fnom, 25°C	+1.65V ±0.4V for 3.3V part
Tristate Function	Input (Pin#2) High (> 0.7V) or open: Output (Pin#4, #5) active Input (Pin#2) Low (< 0.3V): Output disabled in high impedance
Enable/Disable Time	Enable: 2 ms Max; Disable: 200 ns Max

Creating a Part Number **VC75PE-155M520-B A A 1**

- Product Series
- Frequency
- Supply Voltage: B = 3.3V
- Frequency Stability / APR (Min): A = ±50 / ±50 ppm; B = ±25 / ±50 ppm; C = ±50 / ±100 ppm; D = ±25 / ±75 ppm
- Operating Temperature Range: A = 0 to 70°C; B = -40 to 85°C; G = -10 to 70°C; X = Customized Temp Range
- Duty Cycle (see above)

OUTLINE DRAWING