

PECL COMPATIBLE CRYSTAL OSCILLATOR IN CERAMIC LCC PACKAGE - X075PE Series

FEATURES

- RoHS Compliant (Pb-Free), Best Suited for ECL Logic Devices
- Very Low Phase Jitter, Excellent Noise Margin, No Internal PLL
- Leadless Chip Carrier (LCC) Ultra Small Package, Industry de facto Standard Footprint
- Complimentary Output, Tri-state Enable/Disable Standard or Option

SPECIFICATIONS

Frequency Range 10 MHz to 320 MHz

Standard Frequency 10/ 15.625/ 19.53125/ 80/ 100/ 106.25/ 125/ 133.33/ 155.52/ 156.25/ 161.1328 MHz

Input Voltage (Vcc) B = $+3.3 \text{ VDC} \pm 0.3 \text{ VDC}$; C = $+2.5 \text{ VDC} \pm 5\%$

Input Current 88 mA Maximum, depending on frequency and output load

Storage Temperature -55°C to 125°C

Overall Frequency Stability Temperature Range $100 = \pm 100 \text{ ppm}$; $50 = \pm 50 \text{ ppm}$; $25 = \pm 25 \text{ ppm}$

Temperature Range $A = 0^{\circ}C$ to $70^{\circ}C$; $B = -40^{\circ}C$ to $85^{\circ}C$ Standard Stability $50A = \pm 50$ ppm / $0^{\circ}C$ to $70^{\circ}C$

Electric Option (Duty Cycle)

1 = Tristate 60/40%; 3 = Tristate 55/45%; 5 = Tristate 52.5/47.5%

0 = No tristate 60/40%; 2 = No tristate 55/45%; 4 = No tristate 52.5/47.5%

Output Load

50 Ohms to Vcc - 2V or Thevenin Equivalent, Bias Required

Logic "1" / Logic "0" Level (Vcc - 1.02V) Minimum / (Vcc - 1.63V) Maximum

Rise/Fall Time (Tr/Tf) 1 ns Maximum at 20% to 80% Vp-p

Start-up time 5 ms Maximum

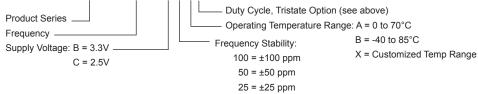
Phase Jitter (RMS, 1 Sigma) 1 ps Max for fj > 1kHz; 0.3 ps Typical for fj = 12KHz to 20MHz

Tristate Function Input (Pin 1) High (> 0.7Vcc) or open: Output (Pin 4, 5) active

Input (Pin 1) Low (< 0.3Vcc): Output disabled in high impedance

Enable/Disable Time 2 ms Maximum - Enable; 200 ns Maximum - Disable

Creating a Part Number XO75PE-155M520-B50A3



OUTLINE DRAWING

