# LOW  PHASE JITTER IN UHF BAND VOLTAGE CONTROLLED  CRYSTAL OSCILLATOR

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## ABSTRACT

Paper presents a new architecture of UHF VCXO in small SMD package for use in optical networking for data communications. Low level of fluctuations of the edges of output signal  (low Phase Jitter), and small physical dimensions satisfy the requirements for oscillators in Clock and Data Recovery (CDR) systems of those networks. We considered the Phase Noise Spectral Density, and suppression of sub-harmonics and their multiples as two key parameters allowing creation of VCXO (or XO) with low Phase Jitter. Out of many possible ways to achieve bulk-wave crystal based VCXO in UHF band we chose the combination of the two. One is based on selection of needed harmonic from the signal of an oscillator operating in 100 MHz to 160 MHz frequency range. The second one is extensive filtering of the signal of desired frequency. This approach allowed to achieve excellent Phase Jitter and Phase Noise performance, as well as long term and temperature stability.

## 1. INTRODUCTION

The UHF band VCXO is an essential component for a number of applications. Low phase jitter of reference signals is a key factor to provide high quality processing of wide-band signals in communications systems. In addition to the low phase jitter the low phase drift is another substantial advantage provided by crystal oscillator. It gives a convenience of application of crystal oscillator in the circuits with a phase alignment and in the efficient CDR units. The requirements for VCXO in optical networks for data communications are defined by the Wavelength Division Multiplex (WDM) technology. In order to separate different wavelength signals each one goes through the CDR operation in its own channel. Hence each channel has its independent VCXO, which synchronizes with the signal's clock frequency in that channel. Number of channels in a limited space put strict requirements for the VCXO size. Phase Jitter requirements are determined by the allowable bit error rate in the channels data stream.

## 2. GOAL SETTING

The target specification of VCXO for application in SONET/SDH networks is well known [1], These requirements allow to synchronize CDR unit and input data stream. Let's consider requirements to this oscillator (for an example at the frequency of 622.08 MHz) with the following parameters:

a)  nominal frequency               622.08MHz;
b)  supply voltage                  +3.3 V±5%;
c)  control voltage                 +1.65±1.5V;
d)  output level                    PECL
e)  operating temp. range           -40 to 85°C;
f)  dimensions                      14x9x6 mm
g)  overall Freq. Stability .        ±30 ppm;
h)  pull ability (APR)              ±50 ppm ;
i)  sub-harmonics  level            -30 dB min;
j)  phase  jitter                   16 ps max.

It is useful, however, to determine what components the integrated Phase Jitter consists of. In our case, when output signal is derived from lower frequency oscillator, not only the Phase Noise Spectral Density contributes to it, but the power level of subharmonics and their multiples as well. For phase shift calculation we can use Formula (1), which defines phase fluctuation dispersion $s_{Dj}^2(t)$ within time $\tau$ through Phase Noise Spectral Density $S_j(f)$ and noise bandwidth ( for SONET/SDH whole jitter bandwidth spans from $f_{min}$ =10 Hz to $f_{max}$ =20 MHz ) [2].

$$s_{Dj}^2(t) = 8 \int_{f_{min}}^{f_{max}} S_j(f)[sin(\pi f t)]^4 df \quad (1)$$

For average phase fluctuation we obtain value

.01 part of the signal period if to substitute values $S_j(f)$=-115 dBc/Hz, $t=1/f_{min}$ =0,1 s in equation (1). It satisfies the SONET requirements. The slope $s_{Dj}^2(t)$ function is positive; therefore jitter at smaller $\tau$ values will be significantly smaller. This statement is correct, however, only for "good" oscillators, which phase noise spectral density may be described by Lissons model [3], and which have not separate lines in spectrum or additional "technical" noise. To define the limits for amplitude of the separate lines in the oscillator signal spectrum, we may apply equation describing modulation of sine-wave signal $u(t)$ with frequency $W_0$ by the harmonic signal with frequency $\alpha$. If the modulation index is designated by letter $\eta$, we obtain following equation for the signal :

$$u(t) = sin[\,W_0 t + h\,sin\,a\,t\,] = \sum_{n=-\infty}^{\infty} J_n(h)\,sin(\,W_0 + na\,)t$$

where $J_n$ is a first order Bessel function. Since $J_1(0,1)$=0,0499, we may consider that the presence the spectral modulation components with level of –26 dB as a consequence of phase modulation with maximum phase deviation of 0.1 radian and vice versa. First order Bessel function, which defines dependence of spectral component amplitude upon modulation index $h$, is linear for the small values of the latter. Therefore, in order to attain phase deviation of 0.01 radian (modulation index equals 0.01), the amplitude of the above mentioned spectral component should not exceed –46 dBc.

### 3. OSCILLATOR ARCHITECTURE

The choice of the crystal frequency is a trade-off between manufacturability, long-term stability requirements, and possibility of the sub harmonic suppression. Considering modern high frequency fundamental crystal processing technology and SONET/SDH long-term frequency stability requirements we have chosen the range of the crystal frequency of 100 MHz to 160 MHz. There are several methods of frequency transformation from above mentioned range into 400 MHz to 1200 MHz range:

    a)   Analogue frequency multiplication
    b)   PLL technique

    c)   Selection of the needed harmonic of the main oscillation frequency from existing harmonics set of the oscillator stage.

It is known that with significant constrains on the physical volume of the oscillator device it's very difficult to achieve high spectral purity of the output signal using first two methods [4,5]. The VCXO development using third method is described in paper [6]. The device has a noise floor of –150 dBc/Hz at the 200 KHz offset of from the carrier, which is typical value for 100÷160 MHz band VCXO. It means that device does not degrade the noise floor far away from the carrier. However, the slope of the single side band phase noise spectral density plot equals 20 dB/decade from 100 KHz to 300 Hz and 30 dB/decade lower 300 Hz. It is a consequence of the loaded crystal quality $Q_L$ degradation due to the influence of the multi-harmonics presence in the oscillator stage. That in turn leads to degradation of the phase jitter in the time intervals from 2 us to 10 ms. In order to reduce the number and the amplitude of the unwanted spectral components we chose the combination of methods a) and c). That resulted in reduction of the amplitude of all unwanted spectral components and the fundamental frequency signal.

### 4. CIRCUIT DESCRIPTION

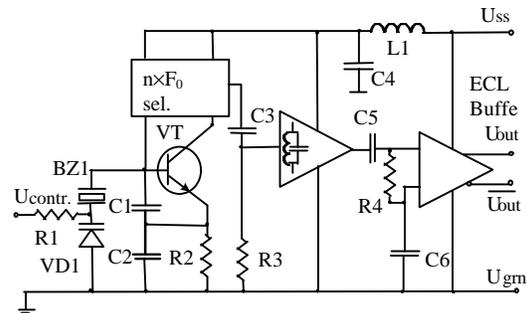The VCXO schematic for 622.08 MHz output frequency signal is shown in Figure 1.



Fig.1. Oscillator basic schematic

The oscillator stage is a Colpitts circuits with a 103.68 MHz fundamental crystal. It has a harmonic selection circuit, which is tuned on the sixth harmonic. It allows reducing the level of unwanted harmonics and thus improving the phase noise performance. The second stage is a narrow band amplifier, which is also tuned on desired frequency of 622.08 MHz. The third

stage buffer is an ECL differential reciever/driver with Enable/Disable feature.

## 4. MEASUREMENT RESULTS

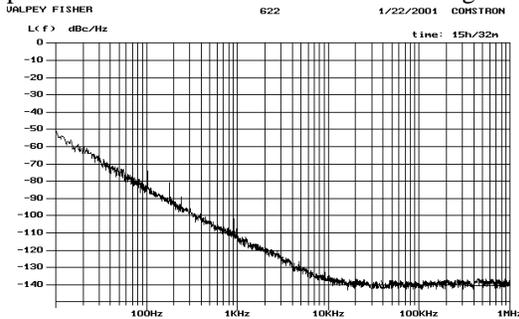Single side band phase noise spectral density plot of 622.08 MHz VCXO is shown on Fig.2.



Fig.2. VCXO phase noise spectral density

As one can see the phase noise level at 10 Hz offset from the carrier is –55 dBc/Hz, -85 dBc/Hz at 100Hz and –140 dBc/Hz on the noise floor, which is reached at about 8 KHz offset. Phase noise floor level is higher by about 10 to 15 dB than that of a conventional fundamental oscillator level. It means that an operation mode of the oscillator stage is more similar to frequency multiplication mode (frequency multiplication by 6 increases the noise level by 16 dB) than to harmonic selection mode. The calculated phase jitter value in the 100 Hz to 1 MHz band is less than 0.2 ps RMS

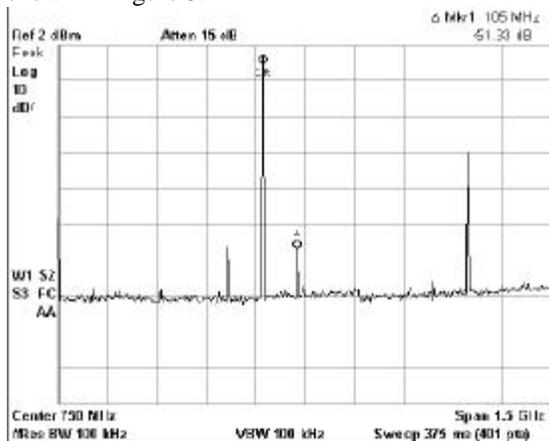The spectrum of VCXO output signal is shown in Figure 3.



Fig.3. The spectrum of VCXO signal.

The suppression of sub-harmonics and their multiples is better than –50 dB with respect to the carrier signal at 622.08 MHz.

The frequency control range is greater than ± 140 ppm, and based on the overall frequency stability of ±

30 to 40 ppm, absolute pull range is greater than ±100 ppm. The tuning linearity is better than ±10 %

High Frequency digitizing oscilloscope HP54120 was used to obtain cycle-to-cycle jitter histogram. The specification of the instrument calls for 2.5 ps trigger jitter RMS. The measured value is close to the specified measurement error, which means that the contribution to that value by DUT is negligible. It confirms our prediction of the cycle –to-cycle phase jitter based on the level of subharmonics.

## 5. CONCLUSIONS

The proposed VCXO architecture has allowed to manufacture an oscillator in a small SMD package (14 x 9 x 6 mm$^3$) and to provide suppression of sub-harmonics and their multiples by more than –50 dB. Oscillator stage design has provided for use of high quality, low aging crystal, and minimization of insertion of "technical" noise, so phase noise spectral density does not exceed –115 dBc/Hz at 1 KHz offset from the carrier, and -140 dBc/Hz on the floor. Total phase jitter value is better than 1 ps over the entire 10 Hz to 20 MHz jitter bandwidth, as well as cycle-to-cycle. Overall frequency stability (including aging) is better than ± 30 ppm.

## 6. REFERENCES